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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,565	09/12/2003	Howard Rhodes	M4065.0570/P570-A	5308

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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,565	RHODES ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *90 and 93-141* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *90 and 93-141* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

2. Regarding communication from applicant dated January 4, 2005, a copy of form PTO/SB/08 is not found in the record. Applicant should re-submit a copy of this information disclosure statement, including a postmark receipt supporting applicants claimed filing date.

Drawings

3. The drawings are objected to because reference 136 in Fig 1 appears to be a misprint, it seems 136 should be replaced with 130.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore:

the "direct contact between said first doped region and said charge storage capacitor", recited in line 9-10 of claim 90, and "connecting an electrode of a charge

storage capacitor directly to said photodiode", recited in line 9-10 of claim 130 (Fig 2: contact between 110 and 199 is through 128 and 130, not direct);

the "storage capacitor is...in contact with said field oxide region", recited in line 13 of claim 108 (Fig 10: 108c contacts 117, which contacts 115);

the "storage capacitor is connected directly to said floating diffusion region", recited in line 12-13 of claim 122 (Fig 10: 166 contacts 168c, no connection shown to 146; 146 not connected to 130, 117 lies inbetween);

the "global shutter transistor" recited in claims 102, 103, 120, and 121 (not shown in any drawing);

the "entire extent of said charge storage capacitor overlies an active area of said photosensor", recited in claim 124 (Fig 11 shows capacitor is not on field oxide, but does not show capacitor overlies a photosensor); and

the "other electrode of said charge storage capacitor is connected to a gate of a transistor", recited in claim 127 (Fig 10 fails to show this);

must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

5. Furthermore, if any claims are amended to indicate "a direct connection" between the claimed storage capacitor and any claimed transistor gate(s), a structural drawing such as Fig 10 clearly illustrating the claimed connection(s) must also be included.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 102, 103, 120, 121 and 124 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

8. Regarding claims 102, 103, 120, and 121, the term "global shutter transistor" is not described in applicant's disclosure; it is only mentioned once in passing in [0070]. There is no drawing to illustrate the structure of a "global shutter transistor" either.

9. Regarding claim 124, it seems that forming the capacitor over the active area of the photosensor would block light from reaching the photosensitive area, rendering the invention inoperable. If the invention could function with the structure claimed in claim 124, applicant must describe how this is possible.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 138-141 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claims 138-141 recite the limitation "said photodiode" in the last line. There is insufficient antecedent basis for this limitation in the claim. Claims 138-141 depend from claim 137 which recites only a photosensor. In interpreting these claims for art-based rejection purposes, the term "photodiode" will be replaced with "photosensor."

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 90-141 are rejected under 35 U.S.C. 102(b) as being anticipated by Rhodes (US 6,204,524).

15. Regarding claim 90, Rhodes discloses (Fig 6-14) a method of forming a CMOS imager (col 8 ln 28-30) comprising the steps of:

providing a semiconductor substrate (116+120; col 8 ln 30-32) having a doped layer (120) of a first conductivity type (col 8 ln 32-33);

forming a first doped region (155; col 7 ln 61) of a second conductivity type (col 7 ln 30-32) in said doped layer, said first doped region being adjacent a field oxide region (115; col 7 ln 25-27);

forming a charge storage capacitor (col 7 ln 65) such that the entire extent of said charge storage capacitor overlies said field oxide region (no extent of 162 lies under 115); and

forming a direct contact (150) between said first doped region and said charge storage capacitor (Fig 5: 150; col 7 ln 61-64, col 8 ln 11-13; forming: col 9 ln 36-50).

16. Regarding claim 93, Rhodes discloses (Fig 10-14) said charge storage capacitor (162) is formed by:

forming a first conductive layer (156; col 9 ln 49-51) over said substrate (col 7 ln 66-67, col 9 ln 28-30, 49-52) including said field oxide region (apparent in Fig 5, 10-14);

forming a dielectric layer (158) over said first conductive layer (col 9 ln 67); and

forming a second conductive layer (160) over said dielectric layer (col 10 ln 14).

17. Regarding claim 94, Rhodes discloses said first and second conductive layers are independently selected (col 10 ln 15-17) from doped polysilicon (col 10 ln 17-18).

18. Regarding claim 104, Rhodes discloses (Fig 8, col 9 ln 8-9, 15-16):

forming a second doped region (126) of said second conductivity type in the doped layer spaced from said first doped region (110) to transfer charge (col 9 ln 9-10, col 7 ln 35-37) from a charge collection area (125+162);

forming a third doped region (130) of said second conductivity type in the doped layer spaced from said second doped region wherein said third doped region effectuates the transfer of charge to a readout circuit (col 9 ln 10-12, col 7 ln 44-50); and

forming a fourth doped region (134) of said second conductivity type in the doped layer spaced from said third doped region wherein said fourth doped region is a drain for a reset transistor (col 9 ln 12-13, col 7 ln 55-56) for said CMOS imager.

19. Regarding claim 105, Rhodes discloses said first conductivity type is p-type (col 7 ln 23-35, col 8 ln 32-34) and said second conductivity type is n-type (col 7 ln 32-33).

20. Regarding claim 106, Rhodes discloses (Fig 8) forming a photogate (102; col 8 ln 46) over said doped layer between said first (155) and second (126) doped regions.

21. Regarding claim 107, Rhodes discloses (Fig 5) connecting an electrode (156) of said storage capacitor to said photogate (156 connects to 102 via 155, 110, and 100; col 8 ln 10-14).

22. Regarding claim 122, Rhodes discloses (Fig 6-14) a method of forming an imager (col 8 ln 28-30) comprising the steps of:

providing a semiconductor substrate (116+120; col 8 ln 30-32) having a doped layer (120) of a first conductivity type (col 8 ln 32-33);

forming a field oxide region (115; col 7 ln 25-28) in said semiconductor substrate;

forming a photosensor (125; col 7 ln 36-37. Formed: col 8 ln 45 – col 9 ln 25) including a charge collection region (110) of a second conductivity type (col 7 ln 31-32), said charge collection region being provided in said doped layer (col 7 ln 30-31);

forming a floating diffusion region (155; floating - not connected to fixed potential) for receiving charge from said charge collection region (col 7 ln 61-64); and

forming a charge storage capacitor (162; col 9 ln 36-37) over said semiconductor substrate (col 7 ln 66-67) so that one electrode (156) of said storage capacitor is connected directly to said floating diffusion region by an electrical contact (150; col 8 ln 10-13).

23. Regarding claim 123, Rhodes discloses (Fig 5) the entire extent of said charge storage capacitor overlies said field oxide region (no portion of 162 lies under 115).

24. Regarding claim 124, Rhodes discloses (Fig 5) the entire extent of said charge storage capacitor overlies an active area of said photosensor (no portion of 162 lies under 125).

25. Regarding claim 125, Rhodes discloses (Fig 5) said charge storage capacitor is formed partially (col 8 ln 20-21) over said field oxide region (left side of 162) and partially over an active area of said photosensor (right side of 162).

26. Regarding claim 126, Rhodes discloses (Fig 14) the other electrode (160) of said charge storage capacitor is connected to ground (col 10 ln 25-28).

27. Regarding claim 127, Rhodes discloses (Fig 5) the other electrode of said charge storage capacitor is connected to a gate of a transistor (there exists a connection pathway from 160 to 108 of 128).

28. Regarding claim 128, Rhodes discloses (Fig 14) said transistor (ex, 128) is part of a three-transistor cell (ex. 102, 128, 132).

29. Regarding claim 129, Rhodes discloses (Fig 5) said transistor (ex, 128) is part of a four-transistor cell (ex. 102, 128, 132, 136).

30. Claims 130-136 are rejected under 35 U.S.C. 102(b) as being anticipated by Han et al. (US 2001/0006238) – hereinafter Han.

31. Regarding claim 130, Han discloses (Fig 4A-4E) a method of forming an imager [0026] comprising the steps of:

providing a semiconductor substrate (202; [0027] ln 1-2) having a doped layer (epitaxial layer of [0027] ln 14-17) of a first conductivity type (p-type);

forming a field oxide region (208) in said semiconductor substrate ([0027] ln 1-4);

forming a photodiode (212) in said doped layer ([0023] ln 5-9);

forming a charge storage capacitor (230; [0025] ln 1, [0028]-[0031]) such that the entire extent of said charge storage capacitor overlies said field oxide region (no extent of 230 lies under 208); and

connecting an electrode of a charge storage capacitor directly to said photodiode by an electrical contact (235; which clearly contacts 212 in Fig 4E).

32. Regarding claim 131, Han does not limit his connection to any particular connection type, therefore, the disclosure encompasses all well-known connection types, including connecting an electrode of said storage capacitor to ground.

33. Regarding claim 132, Han discloses (Fig 4E) the other electrode of said charge storage capacitor is connected to a gate of a transistor (there exists a connection pathway from 235 to 207 of 210).

34. Regarding claim 133, Han discloses said transistor is a transfer transistor (210; [0027] ln 4).

35. Regarding claim 134, Han does not limit his transistor to any particular type ([0024] ln 16-19), therefore, Han's disclosure encompasses all well-known transistor types, including a source follower transistor.

36. Regarding claim 135, Han does not limit his transistor to any particular type ([0024] ln 16-19), therefore, Han's disclosure encompasses all well-known transistor types, including a row select transistor.

37. Regarding claim 136, Han discloses said transistor is part of a three-transistor cell (ex. transfer, reset, and amplification : [0024] ln 11-13, 16-19).

Claim Rejections - 35 USC § 103

38. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

39. Claims 95-103, 108-121, and 130-136 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes in view of Han.

40. Regarding claim 95, Rhodes discloses the method of claim 90, but does not disclose "forming an element of said CMOS imager simultaneously with forming said storage capacitor." Han discloses an analogous CMOS imager [0002] and teaches the method of the current claim ([0015], Fig 4A-4E: [0026] – 0031]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Rhodes by forming the planar capacitor on the same level as the transistor gate, as taught by Han, using the manufacturing method taught by Han; for at least the purpose of reducing the steps of manufacture (Han: [0032]).

41. Regarding claim 96, Han discloses said element is a transistor gate ([0015], Fig 4A-4E: 207, [0026] – 0031]).

42. Regarding claim 97, Han discloses (Fig 4E) connecting an electrode of said storage capacitor to said transistor gate (there exists a connection pathway between 235 and 207).

43. Regarding claim 98, Han discloses (Fig 4E) said element is a transfer gate (207; [0024] ln 11-12).

44. Regarding claim 99, Han discloses (Fig 4E) connecting an electrode of said storage capacitor to said transfer gate (a connection path exists between 235 and 207).

45. Regarding claim 100, Han allows for plural transistors, and does not limit the transistors to any particular type ([0024] ln 16-19), therefore, Han's disclosure encompasses all well-known transistor gate types, including a source follower gate.

46. Regarding claim 101, Han discloses (Fig 4E) connecting an electrode of said storage capacitor to said source follower gate (a connection path exists: [0024] ln 13-19).

47. Regarding claim 102, Han allows for plural transistors, and does not limit the transistors to any particular type ([0024] ln 16-19), therefore, Han's disclosure encompasses all well-known transistor gate types, including a gate of a global shutter transistor.

48. Regarding claim 103, Han discloses (Fig 4E) connecting an electrode of said storage capacitor to said gate of said global shutter transistor (a connection path exists: [0024] ln 13-19).

49. Regarding claim 108, Rhodes discloses (Fig 6-14) a method of forming a CMOS imager (col 8 ln 28-30) comprising the steps of:

providing a semiconductor substrate (116+120; col 8 ln 30-32) having a doped layer (120) of a first conductivity type (col 8 ln 32-33);

forming a field oxide region (115; col 7 ln 25-28) within said semiconductor substrate;

forming a first conductive layer (156) over (no portion is formed under) said field oxide region and said substrate (col 9 ln 49-51);

forming an insulating layer (158) over said first conductive layer (col 9 ln 66-67);

forming a second conductive layer (160) over said insulating layer (col 10 ln 12-14);

patterning said first conductive layer, said insulating layer, and said second conductive layer to form a storage capacitor (col 10 ln 42-45), wherein the entire extent of said storage capacitor is formed over (no extent is formed under) and in contact with said field oxide region (since applicant discloses in Fig 10 contact thorough insulating layer 117, Rhodes Fig 5 contact through insulating layer 106 meets the claim limitation).

50. Further regarding claim 108, Rhodes differs from the claimed invention only in not disclosing "patterning...to form a storage capacitor and an electrical element of said CMOS imager." Han discloses an analogous CMOS imager [0002] and teaches the method of the current claim ([0015], Fig 4A-4E: [0026] – 0031]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Rhodes by forming the planar capacitor on the same level as the transistor gate, as taught by Han, using the manufacturing method taught by Han; for at least the purpose of reducing the steps of manufacture (Han: [0032]).

51. Regarding claim 109, Rhodes discloses (Fig 8, col 9 ln 8-9, 15-16):

forming a first doped region (155; col 7 ln 61) of a second conductivity type (col 7 ln 30-32) in said doped layer and adjacent said field oxide region (115; col 7 ln 25-27);

forming a second doped region (126) of said second conductivity type in said doped layer spaced from said first doped region (110);

forming a third doped region (130) of said second conductivity type in said doped layer spaced from said second doped region and adjacent said electrical element (128, transfer gate of both Rhodes and Han); and

forming a fourth doped region (134) of said second conductivity type in said doped layer spaced from said third doped region.

52. Regarding claim 110, Rhodes discloses said first conductivity type is p-type (col 7 ln 23-35, col 8 ln 32-34) and said second conductivity type is n-type (col 7 ln 32-33).

53. Regarding claim 111, Rhodes discloses said first doped region, said second doped region, said third doped region, and said fourth doped region are doped at a dopant concentration of from about $1x10^{15}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2 (col 9 ln 19-23).

54. Regarding claim 112, Han discloses said electrical element is a transistor gate ([0015], Fig 4A-4E: 207; [0026] – 0031]).

55. Regarding claim 113, Han discloses (Fig 4E) connecting an electrode of said storage capacitor to said transistor gate (there exists a connection pathway between 235 and 207).

56. Regarding claim 114, Han discloses said electrical element is a reset transistor gate ([0023] ln 17).

57. Regarding claim 115, Han discloses (Fig 4E) connecting an electrode of said storage capacitor to said reset transistor gate (a connection path exists: [0024] ln 13-19).

58. Regarding claim 116, Han does not limit his transistor gate to any particular type ([0024] ln 16-19), therefore, Han's disclosure encompasses all well-known transistor gate types, including a source follower gate.

59. Regarding claim 117, Han discloses (Fig 4E) connecting an electrode of said storage capacitor to said source follower gate (a connection path exists: [0024] ln 13-19).

60. Regarding claim 118, Han does not limit his transistor gate to any particular type ([0024] ln 16-19), therefore, Han's disclosure encompasses all well-known transistor gate types, including a row select transistor gate.

61. Regarding claim 119, Han discloses (Fig 4E) connecting an electrode of said storage capacitor to said row select transistor gate (a connection path exists: [0024] ln 13-19).

62. Regarding claim 120, Han does not limit his transistor gate to any particular type ([0024] ln 16-19), therefore, Han's disclosure encompasses all well-known transistor types, including a gate of a global shutter transistor.

63. Regarding claim 121, Han discloses (Fig 4E) connecting an electrode of said storage capacitor to said gate of said global shutter transistor (a connection path exists: [0024] ln 13-19).

64. Claims 137-141 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes in view of Lauxtermann et al. (US 2001/0015831) – hereinafter Lauxtermann.

65. Regarding claim 137, Rhodes discloses (Fig 6-14) a method of forming an imager (col 8 ln 28-30) comprising the steps of:

providing a semiconductor substrate (116+120; col 8 ln 30-32) having a doped layer (120) of a first conductivity type (col 8 ln 32-33);

forming a field oxide region (115; col 7 ln 25-28) in said semiconductor substrate;

forming a photosensor (125; col 7 ln 36-37. Formed: col 8 ln 45 – col 9 ln 25) including a charge collection region (110) of a second conductivity type (col 7 ln 31-32), said charge collection region being provided in said doped layer (col 7 ln 30-31);

forming a floating diffusion region (130; col 7 ln 41-43) for receiving charge from said charge collection region (col 7 ln 61-64); and

connecting an electrode of a {second} charge storage capacitor to said charge collection region by a {second} electrical contact (150; col 7 ln 61-64).

66. Further regarding claim 137, Rhodes differs from the claimed invention in not disclosing plural capacitors; Rhodes does not disclose "connecting an electrode of a first charge storage capacitor to said floating diffusion region by a first electrical contact." Lauxtermann discloses an analogous CMOS imager [0001] and teaches (Fig 2B) connecting an additional capacitor (C1) to the floating diffusion region (55). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Rhodes by connecting an additional capacitor to said floating diffusion region (additional capacitor will differ from first only in being formed above and connected to 130 instead of 155), as taught by Lauxtermann; for at least the purpose of separating the detection and reading processes (Lauxtermann [0006] ln 17-19).

67. Regarding claim 138, Rhodes discloses (Fig 5) said first charge storage capacitor is formed such that the extent of said charge storage capacitor overlies said field oxide region (no portion of 162 lies under 115).

68. Regarding claim 139, Rhodes discloses (Fig 5) a first portion (left side of 162) of said first charge storage capacitor is formed over said field oxide region, and a second portion (right side of 162) of said first charge storage capacitor is formed over an active area of said photosensor (col 8 ln 20-21).

69. Regarding claim 140, Rhodes discloses (Fig 5) said second charge storage capacitor is formed such that the extent of said charge storage capacitor overlies said field oxide region (no portion of 162 lies under 115).

70. Regarding claim 141, Rhodes discloses (Fig 5) a first portion (left side of 162) of said second charge storage capacitor is formed over said field oxide region, and a second portion (right side of 162) of said second charge storage capacitor is formed over an active area of said photosensor (col 8 ln 20-21).

Response to Arguments

71. Applicant's arguments filed on 04/25/2005 have been fully considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800